3. MMU

NXKR\_YoungSikYang

Exported on 2024-02-14 18:29:18

Table of Contents

1 Enable cache 3

1.1 common/cmd\_cache.c for the cache commands 3

1.2 Compile cmd\_cache.c 3

1.3 Enable the cache commands 3

1.4 Enable dcache(disabled by default) 3

1.5 Check icache and dcache are enabled 3

2 Check the speed when the cache is on and off 4

2.1 icache(Instruction cache) 4

2.2 dcache(Data cache) 4

3 Cache in MMU page table 5

4 Cache in memory map 6

# Enable cache

## common/cmd\_cache.c for the cache commands

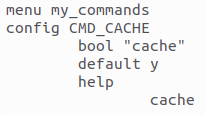
cmd\_cache.c

## Compile cmd\_cache.c

common/Makefile



## Enable the cache commands



## Enable dcache(disabled by default)

This doesn't work



In this file



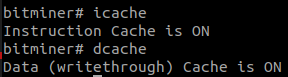
Change this



to this



## Check icache and dcache are enabled



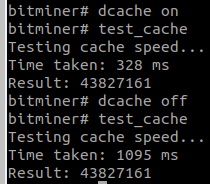
# Check the speed when the cache is on and off

## icache(Instruction cache)

1. icache on
2. mw.l 0x7A000000 0x00FF0000 614400 (This is fast)
3. icache off
4. mw.l 0x7A000000 0x00FF0000 614400 (This is slow)

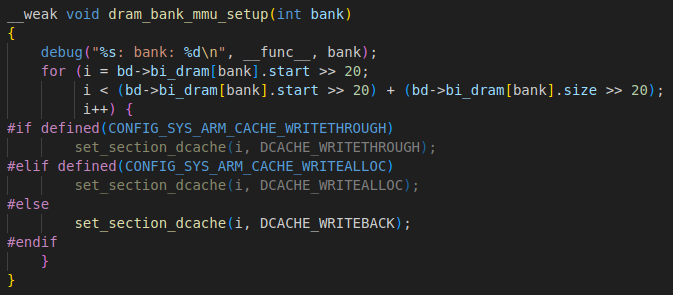
## dcache(Data cache)

|  |
| --- |
| **static** **void** do\_test\_cache(**void**)  {  ulong start\_time, end\_time;  printf("Testing cache speed...\n");  start\_time = get\_timer(0); // Start timer  unsigned long long i=1, result=0;  **for**(i=1; i<=87654321; i++)  result += i % 2;  end\_time = get\_timer(start\_time); // End timer  printf("Time taken: %lu ms\n", end\_time);  printf("Result: %d\n", result);  } |



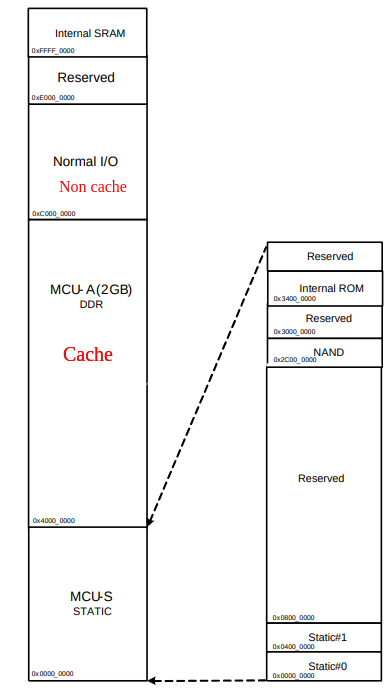
# Cache in MMU page table

arch/arm/lib/cache-cp15.c



This code modifies cache attributes in MMU's page table entries

# Cache in memory map



* SRAM is a cache itself
* DRAM is cacheable for faster speed
* Memory-mapped I/O should be non-cacheable for data consistency (Bits in memory-mapped I/O should not be stored in cache because cache is not mapped to the I/O targets